BANUMATHI.J
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Department of Electronics & Communication Engineering,
Oxford Engineering College,
Trichy-620009

EDUCATIONAL QUALIFICATION

Course	Institution	Board/ University	Year of Completion	Per.	CLASS
M.E (VLSI Design)	Oxford Engineering College	Anna University	2012	8.68 (CGPA)	FWD
BE(ECE)	Shri Angalamman College of Engineering and Tech.	Anna University	2005	74.22	FC
XII	Savithri vidhya sala Hindu Girls Hr.Sec. School,Trichy.	TamilNadu State Board	2001	78.91	FC
X	Savithri vidhya sala Hindu Girls Hr.Sec. School,Trichy	TamilNadu State Board	1999	81.6	FC

WORK EXPERIENCE

Total Experience: 12 Years 4 months

Organization Name	Designation	Period		Experience in years
		From	To	
Oxford Engineering College, Trichy.	Assistant Professor	09.05.2012	Till date	**7** Years
	Lecturer	08.01.2007	08.05.2012	**5** Years **4** months
Total				**12 Years 4 months**

SOFTWARE

- Verilog HDL
- VHDL

HARDWARE

- Altera FPGAs
- Xilinx FPGAs

STRENGTHS

- Programming Skill
- Continuous Learner
- Interested in working as a team
- Adaptable to Working Environment

SUBJECT HANDLED:

- Information Coding Techniques
- Analog and Digital Communication
- Microprocessor and Microcontroller
- Electronics and microprocessor
- Digital Electronics
- Linear Integrated Circuits
- Mobile Communication
- Microwave Engineering
- Radar and navigational Aids
- Computer Networks
- Embedded Systems
- Digital Communication Techniques
- Advanced Microprocessor
- VLSI Design
- CAD for VLSI Circuits
- Testing of VLSI Circuits

ACADEMIC PROJECT

TITLE : FPGA Implementation of CORDIC Algorithm.

AREA : VLSI Design

ABSTRACT:

CORDIC algorithm provides wonderful solution to perform the math intensive operations at the cost of few components like adder, shifter, and multiplexer.Etc. Such math intensive operations are required to perform during the image enhancement phase of finger print re- cognition process. In this paper CORDIC based architecture is proposed to evaluate almost all the trigonometric functions. This is implemented using Cyclone II. Performance of the architecture is analyzed in terms of relative error.

Skill Development Programmes:

Sl. No.	Programme	FDP	STTP	Workshop	Seminar	Conference	Total
1	Number of Programme Attended	10	-	7	2	-	19
2.	Number of Programme Organized	-	-	1	1	-	2

Publications :

Sl. No.	Publications	International	National	Total
1.	Number of Journal	1	-	1
2.	Number of Conference	1	5	6
3.	Number of Book	-		-

Relevant Information:

- Grant Received from CSIR for Three Days Seminar on "Applications of Transforms in signal processing"
- Co - Coordinator of workshop on CSIR sponsored "Network on Chip Architectures"
- Research proposal sent to various funding agencies.
- Guided UG and PG VLSI Projects.